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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/960,125	09/21/2001	Jian Li	884.562US1	6873

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EXAMINER
RAO, SHRINIVAS H

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/960,125	LI ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5,6 and 30-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,5,6 and 30-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 September 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *9/21/01* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

The Application as currently filed does not claim priority from any prior filed application. Therefore currently the earliest available filing date is the U.S. filling date namely 9/21/2001.

Information Disclosure Statement

Acknowledgment is made of receipt of Applicant's Information Disclosure Statement (PTO-1449) filled June 04, 2002 .

The references on PTO 1499 submitted on 06/04/2002 are acknowledged. All the cited references have been considered. However the foreign patents and documents cited by applicant are considered to the extent that could be understood from the abstract and drawings.

Preliminary Amendment Status

Acknowledgment is made of entry of preliminary amendment filed 4/12 /02 . Therefore claims 1,5,6 as amended by the amendment and claims 30 to 42 presently newly added are currently pending in the Application.

Claims 2-4, 7-18 have been can cancelled and claims 19-29 have been withdrawn pursuant to a restriction requirement.

Drawings

The drawings have been objected to by the drafts person for the reasons set out in the enclosed PTO- 948 .

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 39 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 39 the phrase "tungsten via " renders the claim indefinite it is not clear what Applicants' intend to include/exclude from the above recitation.

It is not clear what Applicants' mean by a "tungsten via" , since a via is an opening in a layer, the opening cannot be made of a particular metal or material.

If Applicants' mean a via filled with tungsten then the same must be clearly recited.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 5-6 and 30-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evans et al. (U.S. Patent No. 5,864, 932 herein after Evans) and Yoshimori et al. (U.S. Patent No. 5,468,684 herein after Yoshimori).

With respect to claim1 Evans describes a process for forming a memory device including the steps of:

a first topology over a substrate; (Evans figure 52, col. 13 lines 5 to 24) forming a first ferroelectric memory structure at the first topology and after forming the first topology; (Evans figure 52 # 20) and forming at least one subsequent ferroelectric memory structure over the first ferroelectric memory structure (Evans figure 52 # 30) wherein forming -a first topology includes: includes:
forming a first dielectric layer over the substrate; (Evans figures-52 # 16)
forming a first metal layer over the first dielectric layer: (Evans figures1-52 # 18)
Evans does not specifically describe forming a second dielectric layer over the first metal layer.;

However Yohsimori in figures 1,2 etc. and col. 9 lines 27 to 47 etc. describes forming a second dielectric layer over the first metal layer to prevent degradation of characteristics of the ferro electric material common in the priori art processes and to prevent the cracking and peeling problems associated with the prior art methods of forming ferroelectric capacitors.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Yoshimori's forming a second dielectric layer over the first metal layer in Evan's method to prevent degradation of characteristics of the ferro electric material common in the priori art processes and to prevent the cracking and peeling problems associated with the prior art methods of forming ferroelectric capacitors. (Yoshimori col. 3 lines 10-37).

The remaining limitations of claim 1 are :

forming a first electrode adjacent to the second dielectric lager; (Yoshimori fig1 # 40) forming a second metal layer over the second dielectric layer; (Yoshimori fig.1 #44) forming a third dielectric layer over the second metal lager: (Yoshimori figure 1 # 65, col. 13 lines 27 to 42)forming a third metal layer over the third dielectric layer: (Yoshimori figure 1 # 66)and forming a first via between the first metal layer and the second metal layer.(Yoshimori fig. 1 # 49,50).

With respect to claim 5 , Evans teaches the process according to claim 1, wherein forming a first ferroelectric memory structure further includes:

forming a first ferroelectric-polymer memory layer over the first electrode; and forming a second electrode over the first ferroelectric polymer memory (Yoshimori col. 7 lines 50 to col. 8 lines 50).

With respect to claim 6. Evans describes a process according to claim 1 , wherein forming a first ferroelectric memory structure and forming a subsequent ferroelectric memory structure further includes: forming a first ferroelectric polymer memory layer over the first electrode; forming a second electrode over the first

ferroelectric polymer memory. layer; forming a second ferroelectric polymer memory layer over the second electrode; and forming a third electrode over the second ferroelectric polymer memory layer. (Evans fig. 52, 20, 30 and Yoshimori col. 7 lines 50 to col. 8 lines 50).

With respect to claim 30, Evans describes a method, wherein first ferroelectric oxide memory layer comprising: forming a first electrode over a substrate; ,(Evans figure 52, col. 13 lines 5 to 24) forming a first ferroelectric oxide memory layer over the first electrode; (Yoshimori fig.1 # 42) forming a second electrode over the; (Yoshimori fig. 1 # 44) and forming a second ferroelectric oxide memory layer over the first ferroelectric oxide memory layer, (Yoshimori figure 1) wherein the second ferroelectric oxide memory layer is larger than the first ferroelectric oxide memory layer, (Yoshimori figure 15 , etc.)

. With respect to claim 31.Evans describes the method of claim 30, wherein the second ferroelectric oxide memory layer is formed so that a thickness of the first ferroelectric oxide memory layer is substantially equal to a thickness of the second ferroelectric oxide memory layer and so that a width of the second ferroelectric oxide memory layer is greater than a width of the first ferroelectric oxide memory layer. (Yoshimori col. 10 lines 10-17).

With respect to claim 32, Evans describes the method of claim 30, wherein forming the first ferroelectric oxide memory layer includes forming a ferroelectric oxide memory layer by chemical vapor deposition, spin-on deposition, or physical vapor deposition. (Yoshimori col.11 lines 43).

With respect to claim 33, Evans describes the method of claim 30, the first electrode has a width that is a minimum feature of a photolithography technology, selected from 0.25 micron, 0.18 micron, 0.13 micron, and 0.11 micron. (well known in the art).

With respect to claims 34- 38 Evans describes the method of claim 30, further comprising: forming a via coupled to the first electrode prior to forming the first ferroelectric oxide memory layer and .forming first ferroelectric oxide/polymer memory layer in the cavity. (Yoshimori figures 16 c to 18, etc. col. 14)

With respect to claim 39 to the extent understood, Evans describes the method of claim 35, wherein forming a via includes forming a tungsten via coupled to the first electrode.

With respect to claim 40, Evans describes the method of claim 35, further comprising: forming a second electrode material over the first ferroelectric memory , layer; and forming a second ferroelectric memory layer in the cavity and over the first ferroelectric memory layer, wherein a volume of the second ferroelectric memory layer is greater than a volume of the first ferroelectric memory material.(Yoshimori figs. 16 C to 18).

With respect to claim 41, Yoshimori describes the method of claim 40, further comprising: forming a conductive layer over the second ferroelectric memory layer; planarizing the conductive layer; and patterning the conductive layer to form a third electrode; and forming an interlayer dielectric (ILD) layer over the third electrode; and

forming a third ferroelectric memory layer over the interlayer dielectric layer. (Yoshimori figs. 16 c to 18 and col. 14 line 55 to 67).

With respect to claim 42, Evans describes a method, comprising; forming a structure having a cavity, wherein the structure includes at least one dielectric layer, at least one metal layer, and at least one via; and forming at least one ferroelectric layer in the cavity. (Yoshimori figs. 16 c to 18).

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H. Rao whose telephone number is (703) 306-5584. The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7724.

Steven H. Rao

Patent Examiner

June 12, 2003.

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